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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,057	03/30/2004	Robert M. Reinschmidt	16820P281	7985

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EXAMINER

TAN, VIBOL

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No. 10/815,057	Applicant(s) REINSCHMIDT, ROBERT M.	
	Examiner Vibol Tan	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14, 16-18 and 20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 17, 18 and 20 is/are allowed.
6) ☒ Claim(s) 1-4, 7, 10 and 12-14, 17, 18, 20 is/are rejected.
7) ☒ Claim(s) 5, 6, 8, 9 and 11 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Roper et al. (U. S. PAT. 6,900,663).

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Roper et al. teaches all claimed features in Fig. 3B an apparatus comprising: a plurality of source followers (309, 310), each of the plurality of source followers comprising a pull-down transistor having a source (not labeled), a drain (not labeled), a gate (not labeled), and a bulk terminal (connected to the source terminal); and a plurality of pull-up transistors (304, 305), each of the plurality of pull-up transistors having a source (not labeled), a drain (not labeled), and a gate (not labeled), wherein

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the drain of each of the plurality of pull-up transistors is coupled to the source of a pull-down transistor of the plurality of source followers (at nodes 220 and 221, respectively), to output a plurality of differential signals (220 and 221) via the drains of the plurality of pull-up transistors.

In claim 2, Roper et al. further teaches wherein the bulk terminal of the pull-down transistor is coupled to the source of the pull-down transistor (as shown in Fig. 3B).

In claim 3, Roper et al. further teaches the apparatus of claim 2 wherein the pull-down transistor is a p-channel transistor (as shown).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4, 7, 10, 12-14, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being obvious over Roper et al. in view of Tinsley et al. (US 2003/0085736).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

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in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(I)(1) and § 706.02(I)(2).

In claim 4, Roper et al. teaches all claimed features in Fig. 3B, the apparatus of claim 1; with the exception of teaching a first current source coupled to the sources of the plurality of pull-up transistors; an operational amplifier, coupled to the first current source, to drive the first current source; and a feedback path coupled between the drains of the plurality of pull-up transistors and an input of the operational amplifier. However, Tinsley et al. teaches in Fig. 5, a first current source (I1) coupled to the sources of the plurality of pull-up transistors (M1, M3); an operational amplifier (265), coupled to the first current source, to drive the first current source; and a feedback path (270) coupled between the drains (via R1 and R2) of the plurality of pull-up transistors and an input of the operational amplifier (negative terminal for 265).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Roper et al. with the teachings of Tinsley et al. in order to provide a LVDS driver circuit having means to adjust the current to adjust the common mode of the output up or down.

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In claim 7, Roper et al. teaches all claimed features in Fig. 3B, the apparatus of claim 1; with the exception of teaching a low swing differential pre-driver, coupled to the gates of the pull-down transistors of the plurality of source followers, to drive the pull-down transistors. However, Tinsley et al. teaches in Fig. 4, a low swing differential pre-driver (220), coupled to the gates (IN_1 , IN_2) of the pull-down transistors (M_2 , M_4) of the plurality of source followers, to drive the pull-down transistors.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Roper et al. with the teachings of Tinsley et al. in order to amplify, or may convert to appropriate bias levels before the signals are fed into a LVDS driver circuit.

In claim 10, Tinsley et al. further teaches the apparatus of claim 1, further comprising: a network interface [0003, line 8; networking] including the plurality of pull-up transistors (M_1 , M_3) and the plurality of source followers (M_2 , M_4); and a plurality of transmission lines (not shown) coupled to the network interface, the plurality of transmission lines being driven by the plurality of low voltage differential signals.

Claim 12 corresponds to detailed circuitry already discussed similarly with regard to claim 7.

Claim 13, Roper et al. further teaches the method of claim 12 further comprising reducing body effect on the plurality of pull-down transistors (bulk terminal coupled to source terminal for each transistor).

Claim 14 corresponds to detailed circuitry already discussed similarly with regard to claim 4.

Claim 17 corresponds to detailed circuitry already discussed similarly with regard to claim 4.

Claims 18 and 20 correspond to detailed circuitry already discussed similarly with regard to claim 4.

5. Claims 5, 6, 8, 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. In light of further consideration, the new ground(s) of rejection have been set forth, as discussed above.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Roper et al. and claims 4, 7, 10, 12-14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Roper et al. in view of Tinsley et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER